The VA-DAQ 1.2 test and readout system for the VA/TA chip sets

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Abstract

This document contains one chapter of the ph.D. thesis of the author. It describes a low cost PC-based read-out system for evaluation of new sensors in technologies like Si, CdTe and CdZnTe.
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Chapter 1

A General read-out and test system based on VA/TA

A general low-cost PC-based system for test and read-out VA/TA front-end amplifiers was fully developed by the author during 1998. The complete hardware and an extensive collection of software routines, contained within the VA-DAQ program, were made within this short time span. The short turn-around time and its flexibility in use are mostly attributed to the choice of implementing the code in the graphical programming language LabView, a trade mark of National Instruments. Labview is today one of the most used tools for data acquisition and instrumentation for scientific and commercial applications.

The system has been highly successful and is today used for probe testing, verification and data sheet generation of all VA/TA chips of IDE. The flexibility of the system also allows it to be connected to any high ohmic capacitive (the signal being a charge) solid state detector that can be read out by VA/TA chips.

The success of the system is also demonstrated by being sold to over 20 research institutions, universities and major companies in the field of particle detection throughout the world.

1.1 Introduction to the VA/TA and the VA-DAQ

The VA-family of chips manufactured by Integrated Detector & Electronics AS (IDE) in Norway, contains more than 20 very low noise read out chips normally used as the front-end amplifiers for particle and photon sensors, such as silicon pad- and strip sensors and multi-wire proportional chambers. These sensors find their use both in high energy physics and medical imaging. Even though the VA series of chips are tailored for a variety of applications, as seen from their wide range of possible input charges, input capacitance and peaking times, they have all the same functional schematic. The chips typically have 128 or less parallel input charge sensitive amplifiers. The front-end is based on a pre-amplifier integrator followed by a shaper, both constructed from OTAs as described in chapter 1. Each channel facilitates a separate hold circuitry and the chip has a common
Figure 1.1: The working principle of a VA chip.

The read-out sequence starts with issuing a hold signal, which will open the sampling switches such that each channel holds the signal at the time the hold was issued. At the end of the previous read-out cycle a shift-in bit has been inserted in the chip. This means that the value of the first channel is already at the chip output and ready to be sampled. The chip is clocked and an ADC sampling performed, and this is repeated until all channels have been sampled.

All chips have the possibility to be fully checked on a channel to channel basis without having to connect to the actual input channels (or to a sensor), by using the calibration input mux to inject a charge into any specific channel.

The chip size, typically in the order of 5 mm by 5 mm, allows the sensor to have as low as 50 μm channel pitch. Table 1.1 summarizes parameters for two VA-chips, VA1 and VA-RICH, the chips used in the experiments discussed in chapter 3. Figure 1.3 shows the actual layouts of these two chips. The VA-RICH is a 64 channel chip for bonding to a board, whereas the VA1 is a 128 channel chip for direct bonding to a 50 μm strip detector.

The VA-DAQ system described in this chapter is intended to be used as a general test and read-out system for the whole family of VA-chips. Typical use is in probe testing for verification of chips before they are taken from the silicon wafer, or in testing of read-out hybrids, which typically feature from 2 to 10 chips on small printed circuit boards or thick film hybrids. Since the VA-family, as opposed to the XA-family of IDE, does not facilitate
1.1 Introduction to the VA/TA and the VA-DAQ

Figure 1.2: Channel response and readout sequencing of a VA chip.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>VA-RICH</th>
<th>VA1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>1.2 μm CMOS</td>
<td>1.2 μm CMOS</td>
</tr>
<tr>
<td>Size</td>
<td>5.2mm by 4.5 mm</td>
<td>4.5 mm by 6.2 mm</td>
</tr>
<tr>
<td>Direct detector pitch</td>
<td>not applicable</td>
<td>50μm</td>
</tr>
<tr>
<td>Capacitive load</td>
<td>&lt;10 pF</td>
<td>&lt; 100 pF</td>
</tr>
<tr>
<td>Noise</td>
<td>100 e− + 15 e− /pF</td>
<td>165 e− + 6.1 e− /pF</td>
</tr>
<tr>
<td>Typical gain</td>
<td>~ 8.3 μA/FC</td>
<td>~ 17.9 ± 0.8 μA/FC</td>
</tr>
<tr>
<td>Gain range of chip</td>
<td>10% of mean chip gain</td>
<td>5.4% of mean chip gain</td>
</tr>
<tr>
<td>Pedestal range of chip</td>
<td>4.5% of full range</td>
<td>2.4% of range</td>
</tr>
<tr>
<td>Avg. chip ped. spread</td>
<td>σ &lt; 2.5% of range</td>
<td>σ &lt; 0.8% of range</td>
</tr>
</tbody>
</table>

Table 1.1: Summary of VA-RICH and VA1 parameters.

self-triggering, an external trigger is needed to use VA-DAQ as a read-out system. The VA-DAQ system can accept several types of external triggers. For instance a NIM trigger on a LEMO from a scintillator/photo-multiplier or from a TA-chip, the trigger chip of IDE. The TA-chip can not be used with any VA-chip, since it requires to be bonded to the output of the preamplifier of each VA channel.

The TA contains a very fast shaper (compared to the VA shaper), which is followed by a comparator. A common voltage threshold can be set for all channels. The output of all comparators are ORed together, to give a single trigger for the chip. The TA principle is shown in figure 1.4, and the timing diagram in figure 1.5. The fast TA trigger is, after a delay to match the typical VA peaking time, a suitable candidate for making a hold signal
for the VA. Only a very small time jitter is associated with the trigger for different input charges above the threshold, since the fast shaper has a very fast rise time.

The VA-DAQ was designed to minimize cost and equipment for the user. It is fully controlled with a PC through the parallel port, and the user interface is LabView, the present standard in data acquisition and instrumentation, which features easy graphical programming. The software, consisting of many high level VIs (short for Virtual Instrument), allows the user to measure all fundamental parameters of the chips, such as gain, pedestal and noise profiles. In addition exists a detailed description of the lower level routines, which makes it easy for the user to build his own high level VIs for measuring other
interesting parameters or correlations.

The VA-DAQ system is fitted in a box of approximately 25 cm square and 10 cm height. The general VA-DAQ board is within this box plugged into a board that routes all necessary signals to a connector in the front of the box (The ADAPTER board). Two such ADAPTER boards currently exist, one that emulates the old VA repeater card output, and one recommended for new designs. Both definitions use a 50 pin ERNI connector for 50mil flat cables. The new definition contains all signals needed for a VA-TA hybrid board. The user can have his own ADAPTER board designed, to interface to any preferred connector in the front plate of the VA-DAQ box. Figure 1.6 shows a picture of a VA-DAQ setup, consisting of the VA-DAQ, a PC and a lab-bench power supply. Figure 1.7 shows a picture of the inside of a VA-DAQ system, with the VA-DAQ board and an ADAPTER board visible.

This chapter will try to focus on the more general side of the VA-DAQ software and hardware. Most of the details are described in the appendix.

1.2 A short software description

The main program for controlling the VA-DAQ system, is the LabView VI (Virtual Instrument) called VADAQ.VI. This is a menu driven program from where a large selection of measurements on a VA/TA chip or hybrid can be launched. The most important VIs are:

- **Bias settings.** The VA-chip supplies and biasing can be set. Definition files can be read or written for the chip or hybrid under test, such that the system rapidly can be brought to a specific operating condition.
Figure 1.6: Picture of a VA-DAQ system, showing the VA-DAQ box, a PC and a lab-bench supply.

- **Oscilloscope.** The output waveform from a VA chip subjected to a calibration pulse is shown continuously. The size of the calibration pulse, and biasing voltages and currents can be changed on the fly. This will help the user to find an appropriate pulse-shape response of the chip.

- **Pedestals and noise.** Measures the pedestal and the noise of all channels in a chip. This is done by using a standard read-out sequence, where a hold is issued to the chip and consecutive clocks and samplings of the VA chip output return the pedestal of all channels. The noise is calculated from the spread in the pedestal value of a channel over several read-out sequences. The noise is given after common mode subtraction on a chip basis, and also the common mode for each chip is shown.

- **Gain measurement.** Measures gain and pedestal of every channel in a chip. This is done by fitting the signal response curve (output voltage vs. input charge) for a channel to a n’th order polynomial. The gain is taken as the slope of the profile (and the pedestal as the value of the profile) at zero input charge.
Figure 1.7: Picture of the inside of a VA-DAQ system. It shows the VA-DAQ PCB and an adapter board.

- **Peaking time measurement.** Measures the peaking time for each channel for a fixed input charge. The exact peaking time is found from fitting a polynomial to an averaged oscilloscope picture.

- **Signal profile.** Sweeps through the full range of calibrating pulses to make a signal profile for a channel. Should give an arc-tangent shape with plateaus for both extreme polarities of the calibration step. If these plateaus are not seen, the attenuation of the calibration step should be changed so that the calibration signal covers the full dynamic range of the VA chip under test. A routine similar to this is the core of the gain measurement.

- **Automatic data sheet generation.** Sweeps through a set of tests, defined by the user, resulting in a data sheet in ASCII format describing the results. Acceptance criteria can be set for all important parameters to mark channels as dead or alive. After a data sheet is defined the settings can be committed to a file for later use.
1.3 The use of VA amplifiers

The VA serial readout structure is a very simple scheme, but it has its limitations, compared to the more advanced chips of chapter 4. It can not be used in a dead-time free system, because when a trigger is issued the chip will hold the data from each channel until all channels are multiplexed out. This puts limitations on the readout rate. A system with 1024 channels using a readout clock of about 1 MHz will be busy and not accepting triggers (events/particles) for about 1 ms after the previous trigger.

A certain pre-amplifier/shaper stage can not be optimal for all ranges of input charges (dynamic range), input capacitive load and peaking times. The first decisions for a specific application will be to select a chip which more or less match the dynamic range and capacitive load presented by the detector.

The most important parameter for the system is the S/N-ratio, since this ultimately defines the resolution of the system. In an energy measurement (of photons) this decides the energy resolution, and in a silicon strip detector it will decide the optimal position resolution. To tune the front end will correspond to maximize S/N by scanning all adjustable front-end parameters. These parameters usually includes the current consumption and the feedback resistance in the pre-amp and shaper. The parameters will change the gain, peaking time, amount of undershoot and other features of the pre-amp/shaper output waveform. Unfortunately is this tuning often constrained. The two most typical constraints are the power consumption and the peaking time.

The power consumption is usually limited due to total power budgets, for instance in space applications, or due to limited cooling possibilities. The chip power consumption is almost totally determined by the current in the gain stages (transistors) of the pre-amp and shaper, thus constraining the tuning possibilities.

In a collider experiment the first important setting is peaking time, which is fixed. When a collision occur there will typically take in the order of 1 – 10 μs (a fixed time for each experiment) until we know if this was an interesting collision/event. When the trigger decision comes, typically based on calorimeters or muon spectrometers, the front end chip is told to hold the data. Since we want to sample at the peak of the pulse shape the chip should be optimized to have a peaking time equal to the trigger decision time. Trying to sample off the peak means including extra noise since any time jitter in the system will be mapped into a voltage jitter (noise).

When optimal settings are found for the S/N (measured as the ENC of each channel) other parameters can be measured for the chip. Typically the signal response of a chip is characterized by only two number, being the pedestal and the gain. The pedestal of a channel is defined as its value (DC value) at zero input charge. The gain is given as the slope of the signal response at zero input charge. Due to transistor variation the pedestal and gain are slightly different from channel to channel. In a typical application the user is interested in constraining the channel to channel variation. This is easily motivated by the fact that the serial readout necessarily means quantization of the data by a single ADC with a certain input range. A channel with pedestal or gain far off the typical values is more or less useless since its output does not map the ADC input range. If parameters
are close enough it will often be sufficient to represent the gains and pedestals of a chip with two single numbers (the average pedestal and the average gain), greatly reducing the calculations needed in the later data analysis. It can even facilitate more of the analysis on a DSP close to the front end, reducing the data files dumped to disk for later analysis. For some applications also linearity plays a role. The channel output should be linear for a certain input charge range.

This was a general description on characterizing CSA chips, which motivates the existing measurements available within the VA-DAQ software.

1.4 Overview of chip measurements

The VA-DAQ system front panel is shown in figure 1.8. It is a menu driven program where the required operation can be selected from the menu list on the left hand side. The operations can be divided into four classes. The first menu items are for setting up the system, the next group of items for measuring VA parameters, the third group for measuring TA parameters and the last group for doing detector readout. The detector readout options are for single channel readout or full system readout. The chip supplies and their current draw are shown on the front panel. The supplies are automatically turned off if a defined current limit is passed.

1.5 Setting up the VA-DAQ system

Three menu items exist for setting up the system, Initialize & Calibrate, VA-DAQ setup, and Swap VA Chip/Board.

1.5.1 Startup of system

When the VA-DAQ system is first started one need to initialize it with the menu item Initialize & Calibrate. The system will go through a self test and also calibrate some parameters. Each self test will either give a red or green LED depending on the success. All LEDs should be green for the system to perform properly.

It is not necessary to run this item more than once unless the lab-bench supply for the VA-DAQ or the PC is turned on or off. The system can query for an initialization file during this phase, and the VADAQ.INI file needs to be specified. The file contains the parameters specific for the VA-DAQ system used. If this file is found in the correct directory it will not be queried.

1.5.2 Setting up for VA-TA testing

After the initialization of VA-DAQ one should set up the system for testing a specific VA-TA-board, by the VA-DAQ Setup menu item. Figure 1.9 shows the setup window,
which presents the user with several options. The menu items on the left could more or less be run in the listed order from top to bottom to setup the system.

The first menu item, **Calibrate VA Current**, is used to calibrate the current used by the VA chip/board under test. This calibration is needed since also the VA-DAQ board itself has units powered by the same supply as the VA-chips. The currents used by these units should be subtracted in order to get the correct current draw by the chips.

All parameters for putting the VA-DAQ in a specific state for testing a certain VA-board can be put in a file, called a definition file. This file can be retrieved by choosing the menu item, **Read definition file**. When the file has been read the right side of the setup window will show the general parameters given by the file, such as the chip type under test, how many chips on the tested boards and so on. However, the most important parameters are the values of all voltage and current biases and the values of the chip supplies. These can be popped up by selecting the **Setup biasing** item in the setup frame. Here the values of all biases as read from the definition file are listed, and they can be changed. The menu item **Use current bias settings** is very useful. It will take the values currently in the system and fill them in as default values in the tables. For each bias and supply an offset value can be set. If a bias is further from the default value than the offset indicates it is regarded as an error.

Figure 1.8: Front panel of the VA-DAQ software.
After the definition file has been read the system will not apply the values from the file before it is ordered by the user. This is done with the **Force bias & supply** menu item. The result of the forcing will be listed and error messages given if it was not possible to set a bias to a value closer than the offset value indicates. Errors can be caused by chip problems or by the board under test. At later stages it can be interesting to check whether biases and supplies are within the default values set, this can be done by the **Check bias & supply** menu item.

Several of the VI’s in the main menu can change the setup, for instance can the **Oscilloscope** change specific bias values. As long as the new value has not been set to default value by selecting **Use current bias settings**, they will be reset to default by using for instance the **Force bias & Supply**. After playing around with a new board and one is satisfied with all settings, one should push **Use current bias settings** and write a new definition file, using the **Write definition file** menu item.

If one for some reason would like to change a bias or a supply to a new value it can be done by the buttons **Adjust VA biases** and **Adjust VA supplies**. The first one list all bias values of the system in a window, as seen in figure 1.10 for a five chip VA2 hybrid. The user can change a specific bias or force all biases to the values given by the definition, similar to the force program. The user can set the VA chip supplies in the range 1.7 – 2.4 V for the positive supply and the equivalent negative range for the negative supply. The values for the currents listed will only be the actual VA chip currents as long
as the Calibrate VA current has been performed.

Hot swapping of a chip/board under test is vital to speed up testing. This is done by the Swap chip/board button. It will put all supplies, biases and digital lines for the VA chips to ground level. When finished, a re-calibration of the test charge is performed. This is easily motivated, since the injected test charge depends on the actual terminating resistor on the board under test. The attenuation of the of the test charge also includes some jumpers in the back plate of the VA-DAQ system. If these jumpers have been moved, Swap chip/board must be run to re-calibrate. In this case the board does not have to be disconnected.

The last button in the setup menu is called Shape optimization. There exist two possible options, one to scan any bias to find an optimal peaking time and a second to scan any bias to find the ENC and the gain (usually to locate the lowest possible noise). These are described below.

**Peaking time as a function of biasing**

It is sometimes interesting to work with bias values not at nominal settings, for instance to re-tune for another peaking time that better match the application. For instance in a collider experiment the hold time (peaking time) of the chip needs to be set to the first level trigger delay.

In order to find such a setting it is interesting to scan for instance one of the biases, with the others still at nominal value, to see the effect on the peaking time and signal height. This is exactly what this menu item can perform.
For the shape of the VA pulse, the most interesting parameters to scan are the shabias and the vfs. The first controls the amount of current floating in the shaper OTA. Lowering the current will lower the band-width of the OTA, thus increasing the peaking time. The vfs voltage controls the feedback resistance in the shaper, and thus the RC time-constant and the pulse shape.

**ENC as a function of biasing**

This VI allows the user to scan one of the biases and see the effect it has on the ENC and gain. Both ENC and gain are defined as the average over all channels. It is important to note that the test is performed at a fixed hold delay. This is a very important optimization, since the ENC is the single most important parameter of a system.

In order to achieve good noise performance it is important that vfp is as low as possible. This voltage controls the feedback resistance of the front-end OTA. Since this OTA should operate as an integrator, the resistance should be as high as possible. If it becomes too high, nothing will stabilize the DC point of the integrator and the signal response will die. By scanning vfp one can find the voltage knee where the channel dies. To have good noise performance one should select a vfp value 50 – 100 mV above this point.

An alternative way to find a good vfp value will be to alter vfp in the Oscilloscope and look for the vfp point where the signal response dies out, and in a similar way select a vfp value 50 – 100 mV above.

### 1.6 VA measurements

The menu items corresponding to VA measurements are the Channel oscilloscope, Pedestals & noise, Gains & pedestals, Peaking time and Peaks. The oscilloscope looks only at a single channel, while the other measure some parameter for all channels.

#### 1.6.1 VA signal waveform

The VI allows the user to look at a running oscilloscope picture of an user selected channel, by selecting the Oscilloscope from the main menu. The front panel is shown in figure 1.11.

It is possible to select the time window (typically -1 µs to 30 µs) with respect to the time of charge injection to the chip, and it is also possible to select the input charge in fC. The waveform is not the response to a single charge injection, but rather each point on the waveform is found from a separate charge injection. The full waveform is therefore found by scanning the sampling time over the selected time window, sampling at each time-step with a charge injected. The scan interval (time resolution of waveform) is in the order of 250 ns if the COARSE button is set, which is good enough for typical VA waveforms with 2 µs peaking and tails reaching to about 10 µs. If the time resolution is set to FINE, it is in the order of 25 ns and a maximum time window of about 2.5 µs. It can be used to look
Figure 1.11: VA-DAQ oscilloscope showing a typical VA channel response.

at details of the rising edge of VA pulses and to look at waveforms for fast VA chips with peaking times from 75 – 500 ns.

If the user zooms in on the peak by selecting a suitable start and end time, the values on the right side of the screen will indicate the correct peaking time and peak value.

In the lower end of the panel it is possible to adjust any of the chip biases so that an optimum shape can be found.

### 1.6.2 Measuring offsets and their deviation

The VI Pedestals & noise performs a full read-out sequence a certain number of times (runs) indicated by the user. The pedestal (offset) of a channel is taken as its average value over the runs. The raw noise of a channel is defined as the standard deviation of the samples for this channel. For each readout sequence and for each chip a quantity called common mode can be defined, being the average of all pedestals for that chip for that specific readout cycle. The common mode can be subtracted from the raw pedestal data, giving the common mode subtracted pedestals. The channel noise is calculated from the common mode subtracted data, as opposed to the raw channel noise. The standard deviation on the set of common mode values for a chip over all runs is defined as the common mode noise of the chip, also listed on the front panel.

In the case of a Gaussian distributed channel noise and a Gaussian distributed common mode noise, it is easily shown that the total channel noise is the root square sum of the common mode subtracted channel noise and the common mode noise. This result is proved on a general basis in the appendix, as equation B.15.

Figure 1.12 shows the front panel of this VI, with data for a 5-chip VA2 hybrid. Both the noise and the pedestals are listed as voltage levels into the ADC.
Figure 1.12: VA-DAQ front panel for measuring pedestals and noise.

Figure 1.13: VA-DAQ front panel for measuring gains and pedestals.

1.6.3 Gain measurements

The menu item **Gains & pedestals** will measure the gain and pedestal of all channels, its window being shown in figure 1.13. The shown plot is for a 5-chip VA2 hybrid, and it is clearly visible that the 5 chips have slightly different gain.
Figure 1.14: Variation of peaking time as a function of input charge for a VA channel.

In order to achieve a correct result, two single channel tests should be run. These have their own buttons on the front panel called Check peak time and Check signal profile.

It is important that the user has found a suitable hold time, such that the signal response is sampled at the peak. This can be found by the Check peak time. The injected charge will be scanned in the currently set charge range. For each charge point the peaking time and signal height (not subtracting the pedestal) are measured. Two plots are presented, one is the peaking time as function of input charge, the other the signal height as function of input charge. This is shown in figure 1.14.

When a VA chip is used in a real read-out the hold time (peaking time) is fixed and it is therefore important that the peaking time does not change much with the input charge. In the ideal case where the signal response is proportional to $Qt \exp(-t/\tau)$, with $Q$ the input charge and $\tau$ the peaking time, the peaking time should be independent of the input charge. An acceptable spread is about $\pm 200\text{ns}$. This will still give sampling more or less on the flat part of the peak. If the shape is assumed as above a calculation give that the signal height is still 99.5% at time $t = 1.8\mu s$ and $t = 2.2\mu s$, for a peaking time of $2.0\mu s$. Figure 1.14 shows that for positive input charge is the peaking time in the range $1.8 - 2.0\mu s$ for the scanned charge range, and for negative charge a bit flatter, more like $1.75 - 1.85\mu s$. A peaking time matching the typical input charge of the experiment should be used. This
spread over input charge can be compared to the channel-to-channel spread found by the main menu item **Peaking time** described later.

**Check Signal profile** will scan a desired range of input charges (fC) and measure the chip output signal (mV) at a desired hold time. The values are plotted with the input charge along the x-axis and the chip response along the y-axis. The plot is fitted to a polynomial, and the gain of the chip (mV/fC) is defined to be the slope (first order coefficient) of the fit at zero input charge, whereas the pedestal (offset, the channels DC value) is defined as the output signal value at zero input charge (zero order coefficient of the fit). The signal profile is obtained several times for the same channel to get statistics on the accuracy of the gain measurement (%). If the accuracy is not good enough, either the averaging or the number of charge points along the x-axis can be increased. Figure 1.15 shows a typical front panel. The typical signal response is an arcus tangent shape, which is easily fitted to a polynomial as long as the flat plateaus are not included in the fit. The shown plot has defined a too big charge range and the third order polynomial has problems with the plateaus at large input charges. In this case the input range should be limited to a smaller range to get a good fit.

If the two VIs **Pedestals & noise** and **Gains & Pedestals** have been run, the last main menu item, **Niceplot**, can be run. It will present the gain, pedestals and noise for all channels in three plots, with accompanying histograms. This is the VI best suited for printing the important chip parameters. Figure 1.16 shows the plot produced for a five chip VA2 hybrid after it has been optimized for minimum noise, with the constraint that the peaking time should be 2µs. Average channel noise is 64e⁻, when the system noise is subtracted, to be compared to 60e⁻, the lowest possible noise for a single chip according to the VA2 data sheet.
Figure 1.16: Showing channel pedestal, gain and noise for a 5-chip VA2 hybrid. All 640 channels are fully functional.

1.6.4 Peaking time measurements

The menu item **Peaking time** will check the peaking time of all channels. Each channel is pulsed with the same input charge, selectable by the user, and the signal waveform for a certain time range around the peak is obtained. A polynomial fit is done to obtain the peaking time of each channel, which is plotted. Figure 1.17 shows the front panel.

1.6.5 Peak measurements

The **Peaks** menu item can be used to check the full dynamic range of all channels in a VA chip. Two input test charges can be defined for injection to the chip under test. Typically one selects a big negative charge and a big positive charge. The signal height for each of these two for all channels is shown in two plots. This can be used to check the full dynamic range of the channel, since the gain measurement itself usually only selects a more or less linear part of the arcus tangent shaped total channel response. If the two input charges are selected to be on the two plateaus of the arcus tangent shape, the difference between the two plots is the full output range of the channels.

1.7 TA measurements

The interesting feature to measure for a TA chip is the channel-to-channel variation of the charge needed to have the channel trigger, once a specific threshold voltage is applied to
Figure 1.17: Peaking time of all 128 channels of a TA1 chip. The peaking time is in the range 1.0 to 1.1 \( \mu s \). Channel 43 is a dead channel.

(the comparator inputs of) the TA. The spread should be small to ensure that particles (for instance photons) have the same absolute energy threshold regardless of what channel the particle should hit. The VI TA charge scan will measure the trigger charge for each channel for a specific threshold voltage.

In addition it is interesting to look at the linearity of each channel. This is done with the TA voltage scan which is a single channel measurement. Both menu items are described below.

### 1.7.1 Threshold charge vs. voltage

Figure 1.18 belonging to the menu item TA voltage scan shows a scan for a single channel of a TA1 chip. We see that the trigger charge in the threshold voltage range of 15 – 50 mV is linear. For the specific channel a TA threshold of about 40 mV is needed to set the trigger level to 3.6 fC, which is a signal of a MIP in 300 \( \mu m \) of silicon. This VI is typically used to check the linearity of the charge trigger level versus the set voltage threshold, and to have a feeling for what threshold voltage to set to obtain a certain trigger charge level.

When this VI is run only the specific channel under test is enabled to trigger. This is
Figure 1.18: Trigger charge level as a function of TA threshold for one channel of a TA chip.

done by downloading a mask to the TA where only one channel is set to trigger.

1.7.2 Trigger charge level

The TA charge scan will for all channels find the necessary injected charge to trigger the chip. This is done at a fixed TA threshold voltage. Figure 1.19 shows this plot for a TA1 chip. It shows that for a set threshold of 53 mV the trigger charge needed is in the range 2.9 - 3.8 fC for all channels except for channel 43, which is dead. The charge range to scan, from 1 to 7 fC in plot 1.19, should be selected to be a wide charge range around the expected average trigger charge, which here is 3.4 fC.

Two other interesting buttons exist. One is the Set threshold button, which allows one to set the TA threshold voltage. The other is the Single channel button, used to perform a more detailed test of a single channel. It is this single channel test that helps the user to select a good charge range to scan, and the use of this test is described below.

Single channel trigger level

This VI operates on a rather low level, offering several possibilities of experimenting with the TA trigger for a specific channel. The window associated with this test is shown in figure 1.20. Three buttons on the left will allow the user to define a certain input charge range to scan, Set charge, a TA threshold voltage Threshold and to define the TA mask, Manual mask.

The Manual mask allows one to enable certain channels for triggering. Typically you
Figure 1.19: Trigger charge level at a given threshold for all channels of a TA1 chip.

Figure 1.20: Trigger probability of a given channel as a function of the input charge.

should only enable the channel you want to test. It is also possible to select what polarity you want the chip to trigger on. This polarity is by default set to positive if the present TA threshold voltage is positive, and to negative if the voltage is negative.
When the VI is run it will for each charge in the selected range pulse the VA-TA board a certain number of times, given by the parameter 'Smpls/charge'. The VA-DAQ system will count how many of these pulses that actually gave a TA trigger in response, to build the lower plot that shows the trigger fraction in percent for the scanned charge range. The trigger charge associated with the set TA voltage is given by the x-axis charge at the point where the trigger probability crosses 50%. Figure 1.20 (lower left) shows the trigger charge to be 4.2fC at a TA voltage threshold of 47 mV. The observed plot should be that of an error function, width the sharpness of crossing from 0 to 100% trigger efficiency giving the noise of the trigger channel.

A feature of the TA chip should here be mentioned. If the charge range is selected including both polarities one can often see that triggers are returned for the 'wrong' polarity as long as the charge is big enough. This only implies that the fast shaped TA pulse into the comparator has a small undershoot and then an overshoot, which, when the total charge injected is large, can create a comparator trigger.

1.8 VA-DAQ as a readout system

The last group of menu items is for using the VA-DAQ system as a read-out system. Two menu items, Single channel readout and Full readout exist. The first one is typically used to get a high rate system, in the order of 10k events per second. A single channel readout can not give results as good as reading out the full system. This is due to the fact that the common mode noise cannot be removed without reading out several channels. The full channel readout will give a maximum readout rate of about 32kHz/channel on a typical equipped 1998 PC running Windows-95. This amount to about 250 events/s for a 128-channel readout system.

Both readout possibilities are otherwise very similar, and only full readout will be described here. The front panel for Full readout is shown in figure 1.21. It should be stressed that the data presented on the screen always will be raw data before any pedestal and common mode analysis have been performed.

The collection of data is divided into data collection cycles. The first part of setting up this VI will be to select the acquisition time for each cycle, and also the maximum numbers of events allowed in each cycle, in the shown plot these are 1000 ms and 1000 events, respectively. The last requirement is necessary to minimize the amount of RAM used by the arrays. If the arrays become too big, the PC will have to do swapping of data between RAM and disk, which will slow down the data collection. Acquisition times should maximum be half an hour. Another reason to divide the acquisition into cycles is to reduce time used to update the screen. The screen is only updated at the end of each cycle.

The second part of the setup will be to define the number of data collection cycles to be started when the RUN button is pushed, in the shown plot this is 100 cycles. A run can be stopped before all cycles are completed by pressing the STOP button. The RETURN button will return to the main VA-DAQ panel. The actual plot also shows
that dumping of raw data to file is enabled, meaning that a file with raw data collected is
written at the end of each cycle. The actual file dumping can be disabled, typically done
under the evaluation phase of a new setup, and in this case the number of cycles is set to a
large number, such that one does not need to constantly start acquisition with the RUN
button. The acquisition time should be set short so that the screen is often updated. For
data taking to file, longer acquisition time for each cycle is better, reducing the time used
to update the screen and other unnecessary tasks.

The data files contain raw 16-bit signed ADC values for each channel from each event.
There are no markers in between each event, so the file contains \( N_{\text{events}} \times N_{\text{channels}} \) signed
16 bit integers. An index file will be written to the same directory as the raw data files,
showing the time the cycle was started and the amount of events in each data file.

Three graphs on the panel allows the user to have a visualized picture of the continuous
data collection. The upper left one shows all values in a specific channel (here channel
number 5) for all events of the last acquisition cycle. This shows a rather flat plot with 6
spikes. These spikes are the times when the trigger was associated with this specific channel
and are thus real signals. Most of the time it is however some of the other channels that
trigger and we see just the pedestal value in this channel. The pedestal is seen to be just
above 0 mV, while the largest signals are around 400 mV.

The upper right graph shows the last event of the 186 events of the last cycle. We see
that clearly channel 12 has a big signal and must have been the channel that gave a trigger
for this event. The signal is around 400 mV. For the other channels that did not trigger
we only see the pedestal value.
The last graph is a histogram for one of the channel, here number 5. This histogram accumulates data from all cycles since the run started. On the left it is seen that this histogram contains data from 41 cycles (the run will continue to 100) and so far there are 7720 entries in this histogram. The data sample from each event is scaled by the constant 'Signal \rightarrowhistoscale' and offset such that zero value ends up in bin number 'Zero signal bin'. The by far biggest peak is seen around bin 100, being all the events for channel 5 when it was not the triggering channel. The peak is therefore indicating the pedestal value of this channel. The peak around bin 238 is however associated with the Am-source used. One clearly see that the threshold voltage is set such that signals corresponding to lower than bin 145 will not trigger the TA. The width of the pedestal peak in the histogram can be used to define the raw channel noise before any common-mode subtraction routines have been used. It should be stressed that the histogram is not written to file, only the raw ADC data is written.

The user can write their own program to analyze the raw data files. Additional programs, not integrated into the VA-DAQ software, exist to analyze such raw data files. It will read in the data files, do pedestal and common mode subtraction on the data, and build histograms for each channel. Various cuts on the quality of each event can be set, and also the histogram size can be altered. Scaling and offset coefficients map the raw ADC values into a specific histogram bin. Measurements can be performed on the energy histograms, for instance to measure the energy resolution (%) of peaks in the spectrum. The figure 1.22 shows the result of a very simple analysis program used on data collected by a 32 channel VA-TA system connected to a silicon pad detector. The sensor was radiated with an $^{241}$Am source, which radiate 59.5keV photons. The VA-TA system was confined in an aluminum box and the sensor radiated through a window from the top. The figure shows the energy spectrum for one of the channels, and the Am-peak is easily located around bin 515. Bin 100 in the histogram refers to 0keV, and again shows a peak due to the pedestals. The width of the pedestal peak gives the noise in a channel after common mode subtraction since the analysis do common mode subtraction. The plot in the lower right corner of the figure reveals the energy resolution of the Am-peak and it is seen to be in the order of 2.8% FWHM for most channels.

In figure 1.23 the spectrum for one of the channels is shown. The pedestal peak has been removed and the x-axis scaled to show the energy in keV. The energy resolution of the Am-241 peak is about 2.8%. The threshold for this channel of the TA chip is around 20keV. Closely below the sensor the bottom of the aluminum box will give rise to some back-scattered photons. Figure ?? shows the most probable recoil electron energy of about 11.4keV, which is also the maximum allowable energy, giving back scattered photons with a peak at about 48keV. This is seen in the spectrum.

1.9 A description of the hardware

The VA-DAQ system contains 5 functional hardware units. These are referred to as PAR10, SUPPLY, ADC, PULSE and BIAS, each described below. The VA-DAQ is a bus based
Figure 1.22: Pre-analyze of Am-241 data taken with VA-DAQ system.

Figure 1.23: Am-241 spectrum from one pad of a 32 pad silicon detector.

system, and the card contains an 8-bit bi-directional bus, called the VA-DAQ bus. The PARIO unit sits between the PC and the VA-DAQ bus, allowing the PC to read and write to registers belonging to the other units over the VA-DAQ bus. The other units, all containing different analogue functions, are controlled by the state of these read and write registers. The VA-DAQ address space contains 8 readable and 8 writeable registers, making the VA-DAQ a memory mapped IO system. All operations that can be performed with a VA-DAQ system can be boiled down to a series of read and write operations to this IO-space (registers).

The design is implemented on a double Europe card (160 mm x 233 mm). The top schematic and the PARIO interface are found in figure 1.24. A silk print showing com-
Figure 1.24: The top schematic and the PARIO schematic for VA-DAQ 1.20.
Figure 1.25: Silk print showing component placement and dimensions of VA-DAQ 1.20.
Figure 1.26: All 4 electrical layers of the VA-DAQ 1.20, showing from upper left to lower right: the top layer for component mounting, the bottom layer, the ground plane and the power plane.
ponent placement is given in figure 1.25. The VA-DAQ board contains just above 500 components, all mounted on the top side, and almost all being surface mounted. The design is a 4 layered structure. Two signal routing layers and two inner planes used for split ground and split power. Figure 1.26 is a collage showing all 4 electric layers.

A variety of connections to this local bus can be foreseen. The present VA-DAQ system use the parallel port of a PC as the outside world connection. The PARIO unit contains buffering and logic to map the parallel port Compatibility/Nibble-mode protocol for two-way data transport into the VA-DAQ local bus protocol. The low-level software driver on the PC contains all that is specific for the parallel port, such that the user of this driver sees only read and write operations to the VA-DAQ local bus as the possible/allowed operations.

In this way the only changes needed when changing the interface to say USB (Universal Serial Bus) would be to redesign the PARIO unit of VA-DAQ to a USBIO unit and change the driver to translate between USB and VA-DAQ local bus instead of between the parallel port and VA-DAQ local bus.

1.9.1 Parallel Port Interface; PARIO

The PARIO unit is the parallel port interface and uses Compatibility mode (Centronics or standard mode) for byte transport to VA-DAQ, and Nibble mode for the reverse data transport. Both these modes are supported by IEEE1284-1994, which is the industry defined parallel port standard. The schematic is shown in figure 1.24.

The VA-DAQ system has 16 1-byte registers, 8 for reads and 8 for writes. The interface has been designed such that a change to the much faster EPP (Extended Parallel Port) mode easily can be done. In this mode byte reads and writes are both performed in a single ISA bus I/O cycle. In this way at least 500 Kbytes of transfer rate could be achieved, even in the reverse direction, if the ADC is changed to a faster type (like LTC1419) that converts in 1.25 μs. A channel could be read out in approximately 5 μs (or less), compared to the current system where the read-out time is around 30 μs.

In the back end of the VA-DAQ card, access to the internal data bus is available on a 20 pin IDC (standard flat-cable) connector. The 8 data lines, 4 read strobes and 2 write strobes and also 5V digital and ground, are available. This makes it easy to build an extension card. By using a so called long ADAPTER card, the users can have access to the VA-DAQ bus and implement functions specific for their use.

1.9.2 Supply voltage generation; SUPPLY

The schematic for this unit is shown in figure 1.27. The low noise ±2V supplies are generated, based on a schematic originally from the CERN VIKING repeater used for VIKING chips.

Both supplies are monitored, and it is possible to measure the current to about 1 mA and the voltage to about 200 μV. It is possible to select between pot-meter or PC control (via a DAC) of each of the supplies by a jumper. The output of each supply is accessible
to the rest of the system via a software controllable relay. This can be used to avoid latch up during probe testing or to ground lines when swapping VA-boards under test.

In front two optional green light diodes indicates if the ±2 V supplies are on. The intensity of the light indicates the voltage of the supply. About 1.8 V gives weak light while 2.4 V gives strong light.

1.9.3 Input signal selection and sampling: ADC

The ADC schematic is shown in figure 1.28, and it contains a 14-bit ADC called AD7871 from Analog Devices, with an input range of ±3 V. The input is buffered by an op-amp follower, which input is from a 16 channel input multiplexor. The 16 channels are the cards reference voltages (±2.5 V), the VA chip supplies (±2 V), the current draw of the chip supplies, the ±5 V analogue supplies, the VA chip output after being processed by the trans-impedance input stage, the analogue ground, Monitor-A and B and finally 4 general signal inputs. The monitoring information comes from two 16 channel multiplexors, called Monitor-A and Monitor-B, which means that 32 channels of monitoring information, mostly from the biasing (BIAS) part, is available.

When the ADC has finished a conversion it asserts the parallel port –ACK line. Today this is polled by the readout program. A read-out routine being invoked by an interrupt
can be used to process data every time the ADC has finished a conversion.

### 1.9.4 Digital signal generator and analogue test pulse; PULSE

This unit contains several sub-units, as can be seen in the schematic in figure 1.29. One sub-unit generates 8 differential digital signals at VA logic levels. Six of these are general. The two last one are primarily intended to be used for the clock and hold signals of the VA chip. If the VA ±2V are turned off, these lines are at ground levels.

The second sub-unit of PULSE generates the calibration pulse, which can have both polarities and is generated by a fast 8 bit DAC. The calibration pulse needs to be terminated by 50Ω to avoid distortion. If this is the case, the rise/fall time of the pulse should be 20ns or less. The attenuation of the step is performed by jumpers in the back plate of the VA-DAQ box, to allow for the great variety of input charges existing for the VA family. The attenuation jumpers are described in appendix A.

The third sub-unit processes the trigger (the trigger gives the time of the physical event) and generates the necessary hold delay. This delay is in the order of 500ns to 30μs for an external trigger. When the chip is pulsed with a calibration signal (which simulates an event by injecting a charge into a selected VA-channel), one can have delays in the range of about −1μs to 30μs. Here a negative delay indicates that the chip hold is set before the
Figure 1.29: The PULSE schematic for VA-DAQ 1.20.
calibration line is pulsed. In this way the full waveform in the time domain (oscilloscope) of a VA chip can be investigated. The delay is set by a mono-stable, and the various delays are obtained by using a programmable CMOS resistor in the time constant for the mono-stable. Both resistors contain 100 steps, but one of them have a total resistance being 10 times the other. This allows for both the fine and coarse oscilloscope options found in the software.

It is possible to select between several types of external triggers. A NIM trigger can be given via a LEMO input. This input is terminated in 50 Ω. It is also possible to give a single ended TTL trigger, which is terminated in 50 Ω. A differential TTL (or RS422) terminated in 120 Ω is also available. The last trigger is a differential current trigger to be delivered by a TA chip, which is processed by a very fast comparator.

It is also possible to read back a byte of signals as TTL-levels. In addition spare analogue monitoring inputs can be used to read back logic signals at VA logic levels. This is typically used to check the shift out signal of a VA-chip. The advantage of analogue monitoring of digital signals is that the voltage levels of the logic signals are checked.

### 1.9.5 Bias generation and monitoring; BIAS

There are two sub-units in BIAS, one is the generation of biases for the VA chips, and the other is the monitoring of these biases. This is seen in the schematic in figure 1.30. The system can generate 12 biases, all monitored for both voltage and current. For every pair of bias (like BIAS0/BIAS1) a jumper needs to be set on the board to select between positive or negative voltages generated by this pair. This minor inconvenience gives a factor of two better resolution in the setting of a bias voltage. The 8 first biases can be referenced to either the ±2 V supplies or to the reference voltages (±2.5 V). The first alternative is the preferred choice since it grounds all biases when the ±2 V supplies are turned off. Only these 8 first should be used for the standard VA biasing currents and voltages vref, vfp, vfs, shbias, prebias and ibuf.

There are 6 available monitoring channels brought to the ADAPTER board by connector CON-C. These can be used differently from application to application. They can typically be used to remotely sense the value of ground and supply and vfp on the readout card. On the standard adapter boards only one of these are used to sense the threshold voltage for the TA chip, since it is taken not directly from a bias, but first scaled down by a resistor network.

### 1.10 Overview of read and write registers

All bits in the read and write registers are summarized in table 1.2 and table 1.3. The detailed function of each of the bits/signals are explained in appendix A.

The possible analogue values that can be sampled by the ADC is controlled by multiplexers. These are organized in a two-layer structure. The ADC input multiplexor is a 16-to-1 multiplexor, and the signals selected depends on the multiplexors 4-bit address.
Figure 1.30: The BIAS unit performing bias generation and monitoring in VA-DAQ 1.20.
The signals are described in table 1.4, and the address is controlled by the four lower bits of write register 1. Two of the multiplexer inputs are even connected to the output of two other 16-to-1 multiplexers, used for monitoring mostly the biasing part of the VA-DAQ system. The address for these two multiplexors are common and controlled by the four lower bits of write register 3. The signals on these two multiplexors are described in table 1.5.

The naming convention used in table 1.5 is as follows; BIASx are the actual voltages on the bias output lines and BIASxT is measured on the other side of a 470Ω resistor, which allows measuring the current in each bias. CALR is the raw voltage of the calibration step signal before it is attenuated. The CALA is the voltage after the attenuation.
<table>
<thead>
<tr>
<th>Address</th>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>R0</td>
<td>0-7</td>
<td>ADC0-7</td>
<td>Least significant byte of ADC result.</td>
</tr>
<tr>
<td>R1</td>
<td>0-7</td>
<td>ADC1-15</td>
<td>Most significant byte of ADC result.</td>
</tr>
<tr>
<td>R2</td>
<td>0-7</td>
<td>TRLREG</td>
<td>Readable TTL data on adapter board.</td>
</tr>
<tr>
<td>R3</td>
<td>0-7</td>
<td>Unused</td>
<td>Register reserved for future extensions.</td>
</tr>
<tr>
<td>R4</td>
<td>0-7</td>
<td>RREG4</td>
<td>Optional read register on adapter board.</td>
</tr>
<tr>
<td>R5</td>
<td>0-7</td>
<td>RREG5</td>
<td>Optional read register on adapter board.</td>
</tr>
<tr>
<td>R6</td>
<td>0-7</td>
<td>RREG6</td>
<td>Optional read register on adapter board.</td>
</tr>
<tr>
<td>R7</td>
<td>0-7</td>
<td>RREG7</td>
<td>Optional read register on adapter board.</td>
</tr>
</tbody>
</table>

Table 1.3: Summary of read registers in a VA-DAQ system.

<table>
<thead>
<tr>
<th>Address</th>
<th>Signal name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>R+2.5</td>
<td>+2.5V reference voltage</td>
</tr>
<tr>
<td>1</td>
<td>R-2.5</td>
<td>-2.5V reference voltage</td>
</tr>
<tr>
<td>2</td>
<td>VDD</td>
<td>The VA chip +2V supply</td>
</tr>
<tr>
<td>3</td>
<td>VSS</td>
<td>The VA chip -2V supply</td>
</tr>
<tr>
<td>4</td>
<td>I-2</td>
<td>The current in the -2V</td>
</tr>
<tr>
<td>5</td>
<td>I+2</td>
<td>The current in the +2V</td>
</tr>
<tr>
<td>6</td>
<td>MON-A</td>
<td>Data from monitoring MUX A</td>
</tr>
<tr>
<td>7</td>
<td>MON-B</td>
<td>Data from monitoring MUX B</td>
</tr>
<tr>
<td>8</td>
<td>-5V/2</td>
<td>Half the analogue -5V supply</td>
</tr>
<tr>
<td>9</td>
<td>+5V/2</td>
<td>Half the analogue +5V supply</td>
</tr>
<tr>
<td>10</td>
<td>VASIG</td>
<td>Signal from the VA chip</td>
</tr>
<tr>
<td>11</td>
<td>AGND</td>
<td>Analogue ground</td>
</tr>
<tr>
<td>12</td>
<td>SIG12</td>
<td>General signal for user</td>
</tr>
<tr>
<td>13</td>
<td>SIG13</td>
<td>General signal for user</td>
</tr>
<tr>
<td>14</td>
<td>SIG14</td>
<td>General signal for user</td>
</tr>
<tr>
<td>15</td>
<td>SIG15</td>
<td>General signal for user</td>
</tr>
</tbody>
</table>

Table 1.4: Signals on the ADC input signal multiplexor.

1.11 VA-DAQ connector description

The VA-DAQ PCB is equipped with three IDC connectors to facilitate plug-in boards (ADAPTER boards) that map all relevant signals to a connector in the front plate of the VA-DAQ box for the specific VA-hybrid used. These three connectors are named CON-A, CON-B and CON-C, as can be seen in the mechanical drawing showing dimensions, connectors and jumpers. The signals on these three connectors are found in the tables 1.6, 1.7 and 1.8.

The differential output current OUTP/OUTM from a VA-chip has a typical output range (OUTP-OUTM) of ±5 times the ibuf value. The standard ibuf value is 140 µA giving an output range of ±700 µA. The input trans-impedance amplifier of the VA-DAQ system uses 3.3 kΩ resistors giving voltage swings of about ±2.3 V to the ±3 V input range ADC. This input stage was designed by the Cleo-III group to be used for the read-out of
1.11 VA-DAQ connector description

<table>
<thead>
<tr>
<th>Address</th>
<th>Monitor A</th>
<th>Monitor B</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>BIAS0 (TA vs)</td>
<td>BIAS8</td>
</tr>
<tr>
<td>1</td>
<td>BIAS0T</td>
<td>BIAS8T</td>
</tr>
<tr>
<td>2</td>
<td>BIAS1 (vsf)</td>
<td>BIAS9</td>
</tr>
<tr>
<td>3</td>
<td>BIAS1T</td>
<td>BIAS9T</td>
</tr>
<tr>
<td>4</td>
<td>BIAS2 (ibuf)</td>
<td>BIAS10</td>
</tr>
<tr>
<td>5</td>
<td>BIAS2T</td>
<td>BIAS10T</td>
</tr>
<tr>
<td>6</td>
<td>BIAS3 (vref)</td>
<td>BIAS11</td>
</tr>
<tr>
<td>7</td>
<td>BIAS3T</td>
<td>BIAS11T</td>
</tr>
<tr>
<td>8</td>
<td>BIAS4 (vfp)</td>
<td>CALR</td>
</tr>
<tr>
<td>9</td>
<td>BIAS4T</td>
<td>CALA</td>
</tr>
<tr>
<td>10</td>
<td>BIAS5 (prebias)</td>
<td>MON10</td>
</tr>
<tr>
<td>11</td>
<td>BIAS5T</td>
<td>MON11</td>
</tr>
<tr>
<td>12</td>
<td>BIAS6 (shabias)</td>
<td>MON12</td>
</tr>
<tr>
<td>13</td>
<td>BIAS6T</td>
<td>MON13</td>
</tr>
<tr>
<td>14</td>
<td>BIAS7 (TA vth-neg)</td>
<td>MON14</td>
</tr>
<tr>
<td>15</td>
<td>BIAS7T</td>
<td>MON15</td>
</tr>
</tbody>
</table>

Table 1.5: Signals on the two monitoring multiplexors.

the VA-RICH boards. The general input signals are all well protected, and can sustain rather large over-voltages. The VSS is given one more line than VDD, reflecting that most current into the VA chips are in the VSS-AGND loop.

Several other connectors can be fitted to the VA-DAQ system, the details are explained in appendix A, only two will be described here. These are the PC connection and the power supply connection.

**CN64: Centronics connector for parallel port communication**

A standard Centronics cable to the PC is used. For correct load a 3 meter cable is required.

**CN77: VA-DAQ supply connector**

This is a 6-pin connector on a 100 mil grid. The leftmost pin, when the VA-DAQ is viewed from the back, is number 1. The pin-out of the connector is given in table 1.9. All three supplies should be floating, low-noise and linear. The analogue supplies should be 2 A and the digital 1 A. The supplies are listed in table 1.9. The same supply for analogue and digital +5V could be used if not extreme noise performance is required.

**User made extensions to the VA-DAQ bus**

A mechanical description of the ADAPTER boards is found in figure 1.31. In the case of a long ADAPTER board, the VA-DAQ bus extension connector (CON-D) can be used. The pin configuration for CON-D is given in table 1.10. There are two write strobes and four read strobes found on the connector, to be utilized on the ADAPTER board. As write registers 6 or 7, a 74LS574 8-bit flip/flop can be used. This is easily implemented by connecting the data-bus to the data inputs of the LS574, and tying the wanted write strobe to the clock input of the LS574. Reads are just as easily implemented by using a 74LS245. Here the data bus is connected to the B-side of a LS245 (pins 11 through 18),
<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VDIG</td>
<td>+5V digital supply</td>
</tr>
<tr>
<td>2</td>
<td>DGND</td>
<td>Digital ground</td>
</tr>
<tr>
<td>3</td>
<td>TTL SNG</td>
<td>Single-end TTL trigger (120Ω)</td>
</tr>
<tr>
<td>4</td>
<td>DGND</td>
<td>Digital ground (TTL SNG reference)</td>
</tr>
<tr>
<td>5</td>
<td>TTL DIF P</td>
<td>Differential TTL trig. (120Ω)</td>
</tr>
<tr>
<td>6</td>
<td>TTL DIF N</td>
<td>Neg. phase of differential TTL trigger</td>
</tr>
<tr>
<td>7</td>
<td>TANEG</td>
<td>Negative phase of TA trigger</td>
</tr>
<tr>
<td>8</td>
<td>TAPOS</td>
<td>Positive phase of TA trigger</td>
</tr>
<tr>
<td>9</td>
<td>DGND</td>
<td>Digital ground</td>
</tr>
<tr>
<td>10</td>
<td>VDIG</td>
<td>Digital +5V supply</td>
</tr>
<tr>
<td>11</td>
<td>VADIG7B</td>
<td>General VA logic signal, neg. phase</td>
</tr>
<tr>
<td>12</td>
<td>VADIG7</td>
<td>Positive phase</td>
</tr>
<tr>
<td>13</td>
<td>VADIG4B(TESTONB)</td>
<td>VA logic</td>
</tr>
<tr>
<td>14</td>
<td>VADIG4 (TESTON)</td>
<td>pos. phase</td>
</tr>
<tr>
<td>15</td>
<td>VADIG6B(REGINB)</td>
<td>VA logic</td>
</tr>
<tr>
<td>16</td>
<td>VADIG6(REGIN)</td>
<td>pos. phase</td>
</tr>
<tr>
<td>17</td>
<td>VADIG5B(CLKINB)</td>
<td>VA logic</td>
</tr>
<tr>
<td>18</td>
<td>VADIG5(CLKIN)</td>
<td>pos. phase</td>
</tr>
<tr>
<td>19</td>
<td>VADIG3B(SHIFTINB)</td>
<td>VA logic</td>
</tr>
<tr>
<td>20</td>
<td>VADIG3(SHIFTIN)</td>
<td>pos. phase</td>
</tr>
<tr>
<td>21</td>
<td>HOLDB</td>
<td>VA hold signal</td>
</tr>
<tr>
<td>22</td>
<td>HOLD</td>
<td>pos. phase</td>
</tr>
<tr>
<td>23</td>
<td>VADIG2B(DRESETB)</td>
<td>VA logic</td>
</tr>
<tr>
<td>24</td>
<td>VADIG2(DRESET)</td>
<td>pos. phase</td>
</tr>
<tr>
<td>25</td>
<td>VADIG1B(CKB)</td>
<td>VA clock signal</td>
</tr>
<tr>
<td>26</td>
<td>VADIG1(CK)</td>
<td>pos. phase</td>
</tr>
<tr>
<td>27</td>
<td>RD2B0</td>
<td>Bit 0 of read reg. 2</td>
</tr>
<tr>
<td>28</td>
<td>RD2B1</td>
<td>Bit 1, TTL input</td>
</tr>
<tr>
<td>29</td>
<td>RD2B2</td>
<td>Bit 2</td>
</tr>
<tr>
<td>30</td>
<td>RD2B3</td>
<td>Bit 3</td>
</tr>
<tr>
<td>31</td>
<td>RD2B4</td>
<td>Bit 4</td>
</tr>
<tr>
<td>32</td>
<td>RD2B5</td>
<td>Bit 5</td>
</tr>
<tr>
<td>33</td>
<td>RD2B6</td>
<td>Bit 6</td>
</tr>
<tr>
<td>34</td>
<td>RD2B7</td>
<td>Bit 7</td>
</tr>
</tbody>
</table>

Table 1.6: CON-A. 34-pin IDC connector for digital signals and triggers.

the read strobe to the chip enable (pin 19 of LS245) and direction bit (pin 1 of LS245) is connected to +5V digital. To the A-side of the LS245 the 8 TTL-signals that one wants to read are connected.

1.12 VA-DAQ low and mid level software description

All communication between the PC and the VA-DAQ system goes through the hardware driver. The driver is a LabView VI implemented as a Code-Interface-Node (CIN), which means that the actual code performing the IO operations to the VA-DAQ address space,
<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>OUTM</td>
<td>Negative phase of the VA diff.current signal</td>
</tr>
<tr>
<td>2</td>
<td>OUTP</td>
<td>Positive phase of the VA output signal</td>
</tr>
<tr>
<td>3</td>
<td>SIG15</td>
<td>General input signal</td>
</tr>
<tr>
<td>4</td>
<td>SIG14</td>
<td>General input signal</td>
</tr>
<tr>
<td>5</td>
<td>SIG13</td>
<td>General input signal, REGOUT</td>
</tr>
<tr>
<td>6</td>
<td>SIG12</td>
<td>General input signal, SHIFTOUTB</td>
</tr>
<tr>
<td>7</td>
<td>AGND</td>
<td>Analogue ground</td>
</tr>
<tr>
<td>8</td>
<td>VSS</td>
<td>The VA chip -2V supply</td>
</tr>
<tr>
<td>9</td>
<td>AGND</td>
<td>Analogue ground</td>
</tr>
<tr>
<td>10</td>
<td>VSS</td>
<td>The VA chip -2V supply</td>
</tr>
<tr>
<td>11</td>
<td>AGND</td>
<td>Analogue ground</td>
</tr>
<tr>
<td>12</td>
<td>VSS</td>
<td>The VA chip -2V supply</td>
</tr>
<tr>
<td>13</td>
<td>AGND</td>
<td>Analogue ground</td>
</tr>
<tr>
<td>14</td>
<td>VDD</td>
<td>The VA chip +2V supply</td>
</tr>
<tr>
<td>15</td>
<td>AGND</td>
<td>Analogue ground</td>
</tr>
<tr>
<td>16</td>
<td>VDD</td>
<td>The VA chip +2V supply</td>
</tr>
<tr>
<td>17</td>
<td>AGND</td>
<td>Analogue ground</td>
</tr>
<tr>
<td>18</td>
<td>VPOS</td>
<td>The analogue +5V supply</td>
</tr>
<tr>
<td>19</td>
<td>AGND</td>
<td>Analogue ground</td>
</tr>
<tr>
<td>20</td>
<td>VNEG</td>
<td>The analogue -5V supply</td>
</tr>
</tbody>
</table>

Table 1.7: CON-B, 20-pin IDC connector for analogue VA signal, and the chip supplies.

![Mechanical outline of VA-DAQ Adapter boards.](image-url)

Figure 1.31: Mechanical outline of VA-DAQ Adapter boards.
<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>BIAS0</td>
<td>Is default used for TA vls</td>
</tr>
<tr>
<td>2</td>
<td>AGND</td>
<td>Analogue ground</td>
</tr>
<tr>
<td>3</td>
<td>BIAS1</td>
<td>Is default used for VA vfl</td>
</tr>
<tr>
<td>4</td>
<td>AGND</td>
<td>Analogue ground</td>
</tr>
<tr>
<td>5</td>
<td>BIAS2</td>
<td>Is default used for VA vbuf</td>
</tr>
<tr>
<td>6</td>
<td>AGND</td>
<td>Analogue ground</td>
</tr>
<tr>
<td>7</td>
<td>BIAS3</td>
<td>Is default used for VA vref</td>
</tr>
<tr>
<td>8</td>
<td>AGND</td>
<td>Analogue ground</td>
</tr>
<tr>
<td>9</td>
<td>BIAS4</td>
<td>Is default used for VA vfp</td>
</tr>
<tr>
<td>10</td>
<td>AGND</td>
<td>Analogue ground</td>
</tr>
<tr>
<td>11</td>
<td>BIAS5</td>
<td>Is default used for VA prebias</td>
</tr>
<tr>
<td>12</td>
<td>AGND</td>
<td>Analogue ground</td>
</tr>
<tr>
<td>13</td>
<td>BIAS6</td>
<td>Is default used for VA shabias</td>
</tr>
<tr>
<td>14</td>
<td>AGND</td>
<td>Analogue ground</td>
</tr>
<tr>
<td>15</td>
<td>BIAS7</td>
<td>Is default used for vthr-neg</td>
</tr>
<tr>
<td>16</td>
<td>AGND</td>
<td>Analogue ground</td>
</tr>
<tr>
<td>17</td>
<td>BIAS8</td>
<td>Default used to set value of +2 V supply</td>
</tr>
<tr>
<td>18</td>
<td>AGND</td>
<td>Analogue ground</td>
</tr>
<tr>
<td>19</td>
<td>BIAS9</td>
<td>Default used for TA vrc</td>
</tr>
<tr>
<td>20</td>
<td>AGND</td>
<td>Analogue ground</td>
</tr>
<tr>
<td>21</td>
<td>BIAS10</td>
<td>Default used to set value of −2 V supply</td>
</tr>
<tr>
<td>22</td>
<td>AGND</td>
<td>Analogue ground</td>
</tr>
<tr>
<td>23</td>
<td>BIAS11</td>
<td>Default used for twbi</td>
</tr>
<tr>
<td>24</td>
<td>AGND</td>
<td>Analogue ground</td>
</tr>
<tr>
<td>25</td>
<td>MON11</td>
<td>Monitoring, channel 11 in Monitor-B, Default TA threshold</td>
</tr>
<tr>
<td>26</td>
<td>MON10</td>
<td>General monitoring input (twbi monitoring)</td>
</tr>
<tr>
<td>27</td>
<td>MON13</td>
<td>General monitoring input (GND sense)</td>
</tr>
<tr>
<td>28</td>
<td>MON12</td>
<td>General monitoring input (vfp sense)</td>
</tr>
<tr>
<td>29</td>
<td>MON15</td>
<td>General monitoring input (VDD sense)</td>
</tr>
<tr>
<td>30</td>
<td>MON14</td>
<td>General monitoring input (VSS sense)</td>
</tr>
<tr>
<td>31</td>
<td>AGND</td>
<td>Analogue ground</td>
</tr>
<tr>
<td>32</td>
<td>AGND</td>
<td>Analogue ground</td>
</tr>
<tr>
<td>33</td>
<td>AGND</td>
<td>Ground for the calibration signal</td>
</tr>
<tr>
<td>34</td>
<td>CAL</td>
<td>Calibration pulse, (terminate in 50Ω)</td>
</tr>
</tbody>
</table>

Table 1.8: CON-C. 34-pin IDC connector for biasing and monitoring.

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VPOS</td>
<td>The +5 V analogue supply</td>
</tr>
<tr>
<td>2</td>
<td>AGND</td>
<td>Analogue ground</td>
</tr>
<tr>
<td>3</td>
<td>VNEG</td>
<td>The −5 V analogue supply</td>
</tr>
<tr>
<td>4</td>
<td>AGND</td>
<td>Analogue ground</td>
</tr>
<tr>
<td>5</td>
<td>VDIG</td>
<td>The +5 V digital supply</td>
</tr>
<tr>
<td>6</td>
<td>DGND</td>
<td>Digital ground</td>
</tr>
</tbody>
</table>

Table 1.9: CN77. 6-pin supply connector. Pin1 is on the left when the system is viewed from the back.
Table 1.10: CON-D. 20-pin IDC connector for VA-DAQ bus extension to the ADAPTER board.

through the parallel port, is implemented as a C-code program linked to the VI.

The low level library, Lowlevel.lib, contains all functions to manipulate the hardware settings of the VA-DAQ system. An example list is setting hold delays, setting calibration signal size, choosing the analogue value to sample, turn on or off the chip supplies, setting bias values etc. These functions all work in hardware units, like ADC and DAC counts.

The mid level library, Midlevel.lib, more or less performs the same operations as the low level library, but tries to abstract from hardware units to real values like current, voltage and charge. Some of these involve calculations and the use of calibrated constants for the conversion from hardware units to physical units. The library Globconv.lib contains all global variables used in such conversions and also routines to translate between hardware units and physical units. The library Calculate.lib tries to assemble all calculations that are typically needed to achieve this higher abstraction level. Appendix A will list the most important VI's from these libraries.

1.12.1 The VA-DAQ hardware driver

The LabView version used to make the VA-DAQ VIs is version 4.1. The current hardware driver is written for Windows 3.11 and Win95. Common to all VIs that are involved in time sequential requests to the VA-DAQ hardware, are the error input and error output parameters. Each time the driver is called and it cannot perform the specified data fetch,
it will return an error out value that is equal to the error input plus one. The error output of a high level VI will always be the accumulated count of missed samplings that occurred during the run of the VI.

Another motivation for using error in and out nodes on all VIs is that it ensures sequential running without the use of the LabView (or G) construct 'sequence' that usually ruins the possibility to understand the data flow from one glance at the graphical code.

There are four other special inputs in addition to the error input, called Function, Address, Data and Mask. Function is a simple number to select the function one want the driver to perform. Table 1.11 describes the functions that are implemented and inherent to the hardware driver. Only four functions are vital: **Readword, Writebytetoadr, Waitdata** and **Setport.** **Readword** will read a word (16 bit) from the address specified in the Address parameter (even address required). The word is built by reading the least significant byte from read register 'Address' and the most significant byte from 'Address+1' of the VA-DAQ system. **Writebytetoadr** will write a byte to a register specified with the 'Address' parameter. The actual byte written is given by the 'Data' parameter, but only those bits marked by an 1 in the 'Mask' will be altered in the hardware register. The other bits will remain unchanged. **Waitdata** will poll a certain time (100 \( \mu \)s range) for a data ready (ADC finished sampling). If no data ready is received, it will time out with an error. **Setport** is only for initialization, and is used to set the hardware address of the parallel port. In Win3.11 and Win95, the address is 0x378 for parallel port 1.

Some higher level functions are put in the driver to speed up acquisition, since a lot of overhead is removed when the driver is not called for each read/write operation. These functions are not described in the function table for the driver, since they have their own VI's, though these VI's most often contains only a call to the driver.

<table>
<thead>
<tr>
<th>Mnemonic</th>
<th>Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Readword</td>
<td>0</td>
<td>Read a word. LSB at even adr, MSB at odd.</td>
</tr>
<tr>
<td>Readword14ext</td>
<td>1</td>
<td>Read a word, assuming 14bit ADC-value.</td>
</tr>
<tr>
<td>Readwordauto</td>
<td>2</td>
<td>Read and clocks VA and starts new ADC cycle.</td>
</tr>
<tr>
<td>Readword14extauto</td>
<td>3</td>
<td>As above, but assumes 14bit ADC data.</td>
</tr>
<tr>
<td>Writebytecore</td>
<td>1002</td>
<td>Writes, assumes writing enabled.</td>
</tr>
<tr>
<td>Writebyte</td>
<td>1003</td>
<td>Writes, changes to write mode if not.</td>
</tr>
<tr>
<td>Writebytetoadr</td>
<td>1004</td>
<td>Writes a byte to a specific register.</td>
</tr>
<tr>
<td>Writereadback</td>
<td>1005</td>
<td>Writes, and checks actual bus value.</td>
</tr>
<tr>
<td>Dtrdy</td>
<td>100</td>
<td>Returns the ADC conversion status flag.</td>
</tr>
<tr>
<td>Waitrdy</td>
<td>101</td>
<td>Waits, but times out with error if not.</td>
</tr>
<tr>
<td>Waitrdyb</td>
<td>102</td>
<td>Waits for ADC, but times out if not.</td>
</tr>
<tr>
<td>Setport</td>
<td>500</td>
<td>Set parallel port hardware address.</td>
</tr>
</tbody>
</table>

Table 1.11: The most important VA-DAQ driver function code calls.
1.13 Summary

The development of the VA-DAQ system has resulted in a low-cost PC based chip testing and read-out system for the VA-TA chip sets. The VA-DAQ system has shown the ability to measure chip parameters to a high accuracy, and is able to measure noise figures down to the lowest possible values given by the theoretical noise performance on the input transistor. Equally interesting and important is the possibility to measure chip parameters with similar good results based on probe testing.

A development starting with the first multi-channel multiplexed charge amplifiers like BALDER, AMPLEX and VIKING in the mid 80’s has resulted in the VA/TA chips of today. A multitude of technical problems were solved in these years, resulting in chips that are commercially available for a wide range of applications (input ranges and capacitive loads). The chips are highly reliable, and are today off the shelf products, which due to the VA-DAQ system, can be delivered with guaranteed performance based on wafer testing or testing of finished boards. Exact measurements on a large number of chips have been used to find typical values for all important chip parameters.

The flexibility of the VA-DAQ system also allows it to be a read-out system. More than 20 systems have been sold worldwide to universities, research institutes and major companies for test and verification of new semiconductor detectors in materials such as silicon, CdTe and CdZnTe, making it a successful product in the portfolio of IDE AS.
Appendix A

VA-DAQ 1.20 details

This appendix will explain some parts of the VA-DAQ 1.20 system in greater detail. The first section will explain the function of each bit in the write register of the VA-DAQ IO-space. The following section will describe the connectors and jumper settings possible, and the last section will describe the low and mid level software routines.

A.1 Detailed read and write register description

WRITE REGISTER 0: Controls the readout sequence timing.

- Bit 0 - RESBCAL
  RESBCAL is connected to the counter that holds the 8 bit value for the calibration DAC. It is an asynchronous reset that will set the register value to 0 when the RESBCAL=0. This means that in normal operation this bit should be 1.

- Bit 1 - CKCAL
  By clocking CKCAL (first set it to 1 and then to 0) the value of the calibration DAC register will be increased by 1. If the previous value of the register was 255, a clocking will wrap it around to 0. In normal operation this bit should be 0. The register increases its value on the positive edge of CKCAL.

- Bit 2 - INCDEL
  Clocking INCDEL will increase or decrease, depending on the value of the UDDEL bit, the value of the digital pot that controls the coarse hold delay. The internal value of the pot can be clocked to 99 in one end and 0 in the other end. Additional clock pulses after the pot has reached one of the ends have no effect. When the UDDEL bit is high a clocking will increase the internal counter in the pot, and UDDEL low has the opposite effect. The physical hold delay increases when the pot counter decreases, and decreases when the pot counter increases.

- Bit 3 - INCDEL2
  Has the same effect as INCDEL, but controls the fine delay. The fine delay has steps
in the order of 25ns, whereas the coarse delay have time steps of 10 times as much. The same UDDEL bit controls the counter action of this pot, as for the coarse hold delay pot.

- **Bit 4 - UDDEL**
  Controls the direction of the hold delay when INCDEL or INCDEL2 are clocked. See the description for INCDEL and INCDEL2.

- **Bit 5 - ZEROHLD**
  An external or internal trigger will set the hold signal after the programmed delay. To set hold inactive (low) one needs to set ZEROHLD low. The signal is an asynchronous active low reset signal for the chip hold signal. This means ZEROHLD is usually 1 and is given a short 0 pulse to clear the VA-chip hold.

- **Bit 6 - COMPL**
  This bit set means that the value of the external calibration register is inverted (1's complement) by the DAC. If the calibration DAC is forced to end latching while COMPL is high, it will load the inverted value of what is found in the external register. The external register is controlled by RESBCAL and CKCAL, but also by Register 4. Since 'negative' hold delays are allowed for internal triggers, there are only one way to end the continuous latching of the DAC. The DAC will latch on the falling edge of ZEROHLD. To clear an internal trigger can be done as follows, to make sure that TA-triggering works properly. ZEROHLD and CAL is brought low, followed by setting ZEROHLD high again. An accepted TA trigger should always be accompanied by setting CAL. In this way no external triggers can be accepted while INHIBIT is active. If one wants the DAC to latch the inverted value of what is in the external calibration register, COMPL can be asserted before CAL and ZEROHLD go low, and de-asserted at the same time as ZEROHLD goes high. When the next internal trigger starts with CAL going high the DAC will give a calibration pulse that corresponds to a jump from the inverted calibration register value to the calibration register value. If for instance the calibration register is loaded with 14, the DAC will give a calibration signal from DAC-value 241 (255-14) to DAC-value 14, which is a large negative going calibration step-pulse.

- **Bit 7 - CAL**
  On a positive edge of CAL an internal trigger is initiated. To enable external triggers CAL needs to be kept high permanently. See also the discussion on COMPL. Should also be brought high when an external trigger is accepted.

WRITE REGISTER 1: Controls signal selection and power supplies

- **Bit 0-3 - SADR0, SADR1, SADR2 and SADR3**
  This is the ADC input AMUX address. Bit 3 is the most significant bit in the four bit address, that gives the signal source for the VA-DAQ ADC. Depending on this address the ADC can sample the signals listed in table 1.4.
• Bit 4 - POWEN
  This bit controls the +2V and -2V supplies for the VA-chips with a relay. With the bit set these two supplies are disabled. When disabled, all digital VA-chip signals are disabled, and for default system set up, all VA bias voltages and currents.

• Bit 5 - LOADB
  This bit controls the loading of a byte to the calibration DAC. This bit should be high in normal operation. If a specific value needs to be set in the calibration DAC, the following should be done: Set LOADB low, write the wanted data byte to register 4. Finish off with setting LOADB high again. The two other control signals for the calibration DAC, CKCAL and RESBCAL must be inactive during this sequence.

• Bit 6 - CALGEN
  Setting this bit high will trigger the calibration DAC. It is the logical or of CAL and CALGEN that is the real trigger for the calibration DAC. If the calibration DAC pulses or not depends on how it is setup. It must have been setup with different values in its external and internal register. It takes a negative going pulse on ZEROHLD combined with setting both CAL and CALGEN low to enable the calibration DAC for a new pulse.

• Bit 7 - LATCH
  Setting this bit to 0 will enable external TA triggers, 1 will disable them. Take care not to enable triggers except for the time where they are wanted. Default value is 1.

WRITE REGISTER 2: Controls VA logic signals

• Bit 0 - CONVERT
  There are three ways to force the ADC to do a conversion. An internal/external trigger will after a delay assert the hold, which again starts a conversion. As long as hold is asserted new conversions are easily started by using the automatic read in the driver. This is a routine which reads the ADC and starts the new conversion using the clock pulse for the VA. Both methods involves asserting VA signals (hold or ck). The third method uses the CONVERT bit. This bit is usually low. Setting it high (hold must be inactive, which means external or internal triggers must have been cleared) will force the ADC to convert. After the data is ready and read out, CONVERT must be set low again.

• Bit 1 - VADIG1, CK
  The VA clock signal (ck/ckb). The full VA clock signal is a logic OR of this bit and a clock pulse generated when the ADC is read out in an automatic mode. The following 6 signals are general purpose. They are driven as differential signals at VA logic levels and can easily drive a 100 ohm terminator between the two phases. A default use for them has been defined, this is the use they have with standard ADAPTER boards.
- Bit 2 - VADIG2, DRESET
  Default setting is to put DRESET on bit 2.

- Bit 3 - VADIG3, SHIFTIN
  The VA shift in signal. This is the read-out bit of the chip. A clocking of the chip when this bit is active, will insert a read-out bit into the chip. Consecutive clocks will enable a new channel for outputting its value on the VA chip output. One needs to ensure that shift in is active for both edges of the clock pulse in order to have a correct loading of the VA chip shift register.

- Bit 4 - VADIG4, TESTON
  The VA test on signal. When test on is active, the chip can be tested by using the calibration input.

- Bit 5 - VADIG5, CLKin
  Default used for the TA CLKin, which will clock in the disable channel mask and the polarity bit.

- Bit 6 - VADIG6, REGIN
  Default used for the TA REGIN, the shift register data to be clocked in by CLKin.

- Bit 7 - VADIG7
  A general purpose digital signal at VA logic levels.

WRITE REGISTER 3: Controls bias generation and monitoring

- Bit 0-3 - MADR0, MADR1, MADR2 and MADR3 Address for the monitoring AMUXes. Bit 3 is the most significant bit in a 4-bit number. The number sets the channel selected from the two monitoring AMUXes. If the ADC input AMUX selects either Monitor A or B it can read the signals listed in table 1.5.

- Bit 4 - DACCSB (for bias generation DACs)
  Start loading of a bias to the bias DACs by pulling this signal low. Pull it high again at the end of the down-loading sequence.

- Bit 5 - Bit3.5
  Not used. Reserved for future extensions. Should be kept high as default.

- Bit 6 - DACDAT (for bias generation DACs)
  This is the data for the serial down-loading of the DACs.

- Bit 7 - DACCLK (for bias generation DACs)
  This is the serial clock for the DAC down-loading.

REGISTER 4: Calibration DAC value
• Bit 0-7 - DAC-value
  Writing to this register sets the value of the external calibration DAC register. Ma-
nipulations with CKCAL and RESBCAL can change the content of this register. Bit
7 is the most significant bit. The value written to this register is only accepted if the
LOADB bit is low.

REGISTER 5: Reserved for future extensions of VA-DAQ

• Bit 0-7 - Not used
  No physical register is connected to the write register 5 strobe on the VA-DAQ 1.20 card.

REGISTER 6 and 7: Available for user made plug-in extensions to CON-D
On CON-D the 8-bit data bus and write strobes for these two registers are brought out, in
addition to 4 read strobes, +5V digital and digital ground. The use of CON-D is found
under the connector specification sections.

READ REGISTER 0 and 1: Least and most significant ADC bytes
The ADC value is a 14 bit number in two’s complement. To make it a signed 16 bit
number, just copy the uppermost bit (the fourteenth) to the last two upper bits.

REGISTER 2: Readable TTL-byte newline A byte at TTL-levels can be read from
connector CON-A

REGISTER 3: Reserved for future extension to VA-DAQ
No hardware is connected to the read strobe associated with this register. Reading this
register should give a value of 255 since the data bus has a weak pull up to +5V digital.

REGISTER 4-7: Available for user made plug-in extensions to CON-D
See the discussion in the connector CON-D specification.

A.2 VA-DAQ jumpers and connectors (cont’d)
This section describes jumpers and connectors of the VA-DAQ system to a detail not found
possible to include in chapter 2.

A.2.1 VA-DAQ connectors continued
In addition to the three IDC connectors CON-A, B and C, there are also three LEMO
connectors on the front edge of the VA-DAQ system. From the upper left (looking from
above and the front edge upwards) these three connectors are named CN1, CN11 and
CN42.

CN1: NIM-trigger
This LEMO terminates the incoming signal in 50 Ω. The pot meter P1 right below should
be adjusted to a voltage level in between the two logic levels arriving on the LEMO. A
positive edge is accepted as a trigger, as long as the NIM-trigger is the selected trigger.
This is described in closer detail under the jumper settings. Note that this LEMO is placed
on the VA-DAQ board and not on the ADAPTER board. Another LEMO needs to be placed in the front panel to have access to this signal, or a LEMO cable can be inserted through a hole in the front panel. The same apply to the two other LEMO plugs, CN11 and CN42 mentioned below.

**CN11: INHIBIT**
This LEMO-output at TTL-levels is at logic high level from the time where a trigger is accepted until the system is finished processing the data from this trigger. Can be used as an inhibit signal for other electronics involved in the read out. The yellow LED is on while INHIBIT is active.

**CN42: CAL**
This is the calibration step pulse used to induce an input charge in a VA chip, when the chip is run in test mode. This signal is also available on CON-C. The signal should end in 50 ohms, and the signal applied to a typically capacitor of 1.8pF connected to the CAL pad of a VA chip. On the lower edge of the card three connectors are found. CN64 is for the parallel port cable connection, CON-D is for digital extension cards and CN77 is for the VA-DAQ supplies.

## A.2.2 VA-DAQ jumper settings

In the system several 2-pin and 3-pin jumper settings exist. On a 2-pin jumper a jumper does not need to be present, whereas on a 3-pin jumper there needs to be a jumper in one of the two positions. Except for the attenuation of calibration pulse, which is available in the backplane of the VA-DAQ system, no other jumpers are available for the common user.

### Jumpers for attenuation of the calibration output

There are five two pin jumpers for attenuation of the calibration step in the right side of the VA-DAQ back plate. These are stacked next to each other. A jumper should be put on one of these five jumpers. The leftmost position gives no attenuation, and each step to the right gives 6 dB attenuation. In the rightmost position the attenuation will be 24 dB.

To the right of these jumpers, two 3-pin jumper settings are found. Each control a 20 dB attenuation. With the jumper in the left position there is no attenuation and in the right position there is 20 dB attenuation.

### Jumper for additional attenuation of the calibration output

The jumper, CN43, is located in the upper right corner, close to the LEMO for the CAL signal, CN42. This will terminate the CAL signal in 51 ohms before it leaves the VA-DAQ card. Can be used with VA-hybrids without 50 ohms termination mounted, and will then ensure correct operation of the -20dB attenuator. This jumper is not mounted as default in a VA-DAQ system.
Jumpers for external trigger selection

There are four 2-pin jumpers close to each other on the left edge. A jumper needs to be put on one and only one of these four jumpers. Depending on the position of the jumper, a specific external trigger is chosen:

- Jumper on CN44: Selects the NIM-trigger on LEMO CN1.
- Jumper on CN45: Selects the single-ended TTL-trigger on CON-A.
- Jumper on CN46: Selects the diff. TTL-trigger (or RS422 trigger) on CON-A.
- Jumper on CN47: Selects the TA-trigger on CON-A. This is the default setting.

Jumpers for setting polarity and levels of bias signals

The 3-pin header CN58 selects the maximum voltage levels for positive bias voltages (above ground). If the jumper is in the leftmost position the VA +2 V is selected, in the rightmost position the +2.5 V reference is selected. Similar for CN59 but for the −2 V and the −2.5 V. The default is to select the ±2 V supplies as maximum voltage levels.

The 3-pin headers CN56, CN60, CN57 and CN61 are used to select polarity of the biases BIAS0-1, BIAS2-3, BIAS4-5 and BIAS6-7. With the jumper in the leftmost position, positive voltage is selected. As default, the jumper selections are left, right, right and right for CN56, CN60, CN57 and CN61.

Jumpers for controlling the ±2 V supplies

The 3-pin headers CN54 and CN55 controls the +2 V and −2 V supplies, respectively. If the jumper on CN54 is in its leftmost position, the value of the +2 V supply is controlled by the pot-meter just below the header. The same apply to CN55, but for the −2 V supply. If the jumpers are in the rightmost position, the +2 V supply is controlled by BIAS8 and the −2 V supply by BIAS10.

Two and three-pin headers which are not intended for jumpers

Under the ADC, CN49 is placed, on pin1 analogue ground is found and the digital ground on pin2. From the bottom side of the card a wire should be soldered in to connect analogue and digital supplies. With default supplies, where both analogue +5 V, analogue −5 V and digital +5 V supplies are floating with respect to each other, the VA-DAQ needs the two ground planes to be connected in one point only. Somewhere between the ADCs analogue and digital ground pins is the optimal place for this connection. In a system with all three supplies grounded together at the supply-unit, this connection should not be shorted. Such a solution is not considered optimal.

The CN12 footprint on the upper edge, between the LEMO CN11 and CON-B, can be connected to a yellow LED. The left leg is the cathode. This LED will be on when the
INHIBIT signal is active. The best is to drag a twisted pair to a LED housed in a socket in the front plate. The CN23 and CN24 footprints between CON-B and CON-C can be used for two green LEDs. For CN23 the cathode is the left leg and for CN24 the cathode is the right leg. The CN23 LED will be on when the $-2\,\text{V}$ supply is enabled, and the CN24 LED when the $+2\,\text{V}$ supply is enabled. The LEDs could be fitted in the front plate.

A.3 Low and mid-level software description

The low- and mid-level software of the VA-DAQ system is listed in the following subsections. The mid-level and the helping routines in the Calculat.llb (calculational help) and Globconv (Global variables and conversion VI’s) is the starting point for developing own VI’s for measuring other interesting parameters besides those already existing among the menu items.

A.3.1 Low level library; Lowlevel.llb

All low level VI’s, defined to be VI’s that use the hardware driver, is collected in the LabView library Lowlevel.llb. The hardware driver itself is also found in the library. The low level VI’s are grouped into functional units. In addition a few global variables for VI’s in the Lowlevel.llb is found in Lowglobs.VI.

VI’s for analogue signal selection

Setmux - Selects the signal to read from the 46 analogue channels.

VI’s for setting the hold delay

Chgdel - Sets/increments coarse/fine delay.

VI’s for setting the calibration signal size

Chgcal - Sets/Increments the value of the external calibration DAC. Will not affect the value of the internal DAC unless it is transparent at the moment.

Chgpulse - Sets/Increases calibration register value, and makes ready for a cal pulse with Settrg. A quiet mode exist where external/internal value is the same.

VI’s for controlling VA logic signals

Clock - Gives a single clock pulse to the VA chip.

Reset - Resets the digital part of the VA chip.

Shiftin - Resets and clocks a read-out bit into the VA read-out register.

Gotochan - Shifts in a read-out bit and clocks it to the wanted channel.
Settest - Puts the VA chip in or out of test mode.

VI’s for setting the biasing DACs
Setbias - Sets a value of 0-255 in one/all of the twelve biasing DACs.

VI’s for trigger conditioning
Settrg - Generates an internal trigger. Also needed to confirm external triggers.
Clrttrg - Clears an external/internal trigger. Can also prepare calibration DAC for new pulse if wanted.
Pulse - Will pulse the calibration DAC. Will not have any effect on the hold or the ADC sampling as Settrg will. 
Enxttrg - Will enable/disable the possibility of an external TA trigger to VA-DAQ

VI for initializing, cleanup and bus check of the VA-DAQ system
Initdaq - Will put the VA-DAQ system in a well defined startup state.
Clearold - Will reset any set trigger and dump any rubbish ADC data.
Chkbus2 - Will check that all possible bytes can be written and re-read from the bus.

VI’s for read-out of all channels (pedestal read-out)
Pedinit - Initializes for read-out of all channels.
Pedcorex - Reads a number of channels from a VA-chip. Returns pedestal values in mV. The Pedcorex is implemented by calling other low level VI’s. A mid level routine for reading pedestals exist, where all software is inside the driver, making it faster.

VI for enabling/disabling the VA chip supplies, digital signals and biases
Setpow - Turn on or off the +2V/-2V supplies.

VI for down-loading and read back of shift register (TA mask)
Setmask - Downloads and checks a TA mask, using CLKN, REGIN and REGOUT.

VI’s for sampling of the VA output waveform
Waveinit - Initializes for grabbing points on waveforms.
Nwawipul - Reads a point on the waveform at current hold delay and cal-size. Will average over N samples, and also end with the possibility of increasing the cal-DAC value.
Nwaitext - Much like Nwavipul. But will issue a calibrate pulse and let a potential external TA response trigger the ADC readout. Will return how many out of the N runs that gave an external trigger.

Mwaitexi - As Nwaitext but the code inside the driver.

VI's for time delays

Wait1ms - Wait some ms, by performing dummy status reads from VA-DAQ.

Timecore - Is used to find wait time from Settrg to data ready.

VI's for reading analogue values

Nmon - Returns average of several samples with the ADC.

A.3.2 VI's for calculational purpose; Calculat.llb

This is a collection of routines performing various calculations.

VI's for statistics and other calculations

These routines perform various general algorithms.

Addeadar - Merges a list of integer values.

Andarray - ANDs together all elements of a boolean array.

Avgstd - Calculates average and standard deviation of an array.

Convjump - Performs Outarray(i)=Inarray(N-i)-Inarray(i).

Interp - Fits a polynomial to a data set and locates the peak.

Mean - Calculates the mean of a data set.

Nantmean - Returns the mean of a data set if some tests are accepted.

O10in255 - Returns a value 10 off the input, but in the range 0-255.

Ofrange - Returns the indices of the input elements that didn’t pass a cut.

Okarray - Returns an array of elements that do not have the indices mentioned.

Sqsum - Calculates a square sum. Reduces it by square root of the samples.

Trunc255 - Truncates the input to an integer value in 0-255.

Trunc99 - Truncates the input to an integer value in 0-99.

Widecm - Expands an array into a bigger one, with multiple similar elements.

Calculations needed for delays and bias adjustments

The VI's below are not general in the sense that they use global variables specific to VA-DAQ.

Calcdel - Calculates the hardware settings for the wanted hold delay in μs.
Coarseadj - Coarse bias DAC setting to get wanted voltage.
Fineadj - Fine adjust of bias DAC to get wanted voltage.
Truncbias - Truncates a wanted bias voltage into the possible range.

A.3.3 VI’s for measuring and setting real values; Midlevel.llb

The VI’s in Midlevel.llb rely heavily upon global variables, which values have been calibrated once an for all or at every start up of VA-DAQ. The global variables themselves and the VI’s to calibrate them are found in the Globconv.llb

VI’s in Midlevel.llb

- **Calib22** - Measures the two biggest calibration steps after the attenuation.
- **Calibcl2** - Measures all 256 calibration steps before the attenuation.
- **Curslope** - Measures the current-slope (mV/μA) of a bias.
- **Getgain2** - Measures the gain of all channels.
- **Getpeaks** - Measures the signal values at two defined peak calibration steps.
- **Getped2** - Measures the pedestal values of all channels.
- **Getsout** - Checks if the shift out circuitry of the VA chip is working.
- **Measbias** - Measures the voltage and current in the biases.
- **Measpow** - Measures the voltage and current in the ±2V supplies.
- **Npedcs** - The core in the pedestal calculations, like in Getped2.
- **Readbiv** - Returns the voltage and current for one of the biases.
- **Readmon** - Reads the value of the 6 general monitoring channels.
- **Seta8biv** - Sets the 8 first biases as close as possible to the wanted voltages.
- **Setbapv** - Tries to set biases and supply to the wanted voltage/current.
- **Setbiv** - Sets a bias voltage as close as possible to the wanted voltage.
- **Setdel** - Sets the hold delay as close as possible to the wanted value.
- **Thcore** - Measures the threshold input charge for the TA.

A.3.4 VI’s for global variables, calibration and conversion; Globconv.llb

The VI’s in this library are grouped into three different categories. One category is the global variables, the next contains the routines for calibrating the VA-DAQ system, whereas the last category contains the VI’s for converting measured quantities like ADC counts into real quantities like mV or μA.
VI's containing global variables

Globadc - Global variables for the ADC.
Globbia - Global variables for biasing.
Globcal - Global variables for the calibration step.
Globfix - Global variables measured once for the entire system.
Globsof - Global variables for software, contains file paths.
Globaut - Global variables common to automatic testing.
Globautb - Global variables for biasing part of automatic testing.
Globautg - Global variables for the general part of data sheet for automatic testing.
Globautm - Global variables for the misc. part of the automatic testing.
Globautn - Global variables for the noise part of the automatic testing.
Globautp - Global variables for the pedestal part of the automatic testing.
Globauts - Global variables for the gain part of the automatic testing.
Globautt - Global variables for the peak/range part of the automatic testing.

VI's for calibration

Clbadc - Calibrates the ADC.
Clbbias2 - Calibrates the bias voltages.
Clbcal2 - Calibrates the step pulse (the calibration step).
Clbpow - Calibrates the supply voltages.
Cltim - Calibrates the hold timing.
Biasctr2 - VI used by Clbbias2.
Powctrl - VI used by Clbbias2.
Tuneim2 - Calibrates the Wait1ms VI.

VI's for conversion between different units

Adcmv - Converts ADC counts to mV.
Dadcmv - Converts an ADC count difference to mV.
Madcmv - Converts an array of ADC counts to mV.
Dmadcmv - Converts an array of ADC count differences to mV.
Mvib - Converts a sensed mV difference into current in uA.
Mnvib - Converts an array of mV differences into current in μA.
Mvis - Converts a sensed mV difference into a supply current in mA.
A.4 Automatic testing

VI’s for defining setups and launching automatic tests are found in the two libraries; Adeffile.llb and Automeas.llb. The Adeffile.llb contains everything necessary to read and write definition files for setup of VA-DAQ for a certain chip/board. Automeas.llb contains all VI’s for setting up the automatic testing and other parameters, the VI’s that are performing the actual measurements and the VI’s for writing the result to file.

A.4.1 VI’s in Automeas.llb

The main VI for setting up a system definition and automatic data sheet generation is the Automeas.vi.

Setup of parameters

The setup of parameters, both setting up VA-DAQ, defining tests and cuts and how to write result to files are done by the following VI’s. Each item will pop up its own front panel to set up the parameters.

Geneinfo - Define the general parameters for the tested board.
Biasinfo - Set up the biasing part of the definition.
Pedinfo - Set up the pedestal part.
Noiinfo - Set up the noise part.
Gaininfo - Set up the gain part.
Peakinfo - Set up the signal peak part.
Miscinfo - Set up general tests on chip basis. (Like functionality of shiftout).
Biasipar - Helping routine for Biasinfo.
Gainipar - Helping routine for Gaininfo.
Peakipar - Helping routine for Peakinfo.

Doing the automatic test

Most measurements called have their VI’s in Midlevel.llb. The measurements are stored in global variables, one global VI for each of the -info (like Biasinfo) VI’s in the previous section.

Doauto - The VI launching the wanted measurements. Front panel to show progress.
Biastest - Checks if biasing/supply within specifications. Will return an error string.
Biaschk - The core of the bias/supply checking.
Writing the results of automatic testing to file

Wrtauto - The main VI, a front panel will show the test result.
Genewrt - Will write the general part of the data sheet.
Biaswrt - Will write the biasing part.
Pedwrt - Will write the pedestal part.
Pedwrtfe - Helping routine for pedwrt. (For each chip).
Pedwrtco - Helping routine for pedwrt. (Common for all chips)
Noiwrt - Will write the noise part.
Noiwrtfe - Helping routine for noiwrt. (For each chip)
Noiwrtco - Helping routine for the noiwrt. (Common for all chips)
Gainwrt - Will write the gain part.
Gaiwrtfe - Helping routine for gainwrt. (For each chip)
Gaiwrtco - Helping routine for gainwrt. (Common for all chips)
Gaiwrthe - Helping routine for gainwrt. (Header part)
Gaindev - Helping routine for gainwrt. (Gain deviation).
Peakwrt - Will write the signal peak part.
Peawkwrtco - Helping routine for peakwrt. (Common for all chips).
Miscwrt - Will write the miscellaneous tests part.
Wrtdead - Helping routine common for these routines.
Wrtallp - Helping routine common to these routines.

A.4.2 VI’s in Adeffile.1lb

The VI’s for writing the definition file

Autwfile - Main VI for writing the definition file, calls the ones below.
Autwhead - Writes the header of the definition file.
Autwgene - Write the general info for data-sheet generation.
Autwbias - Write the biasing part of the data-sheet generation.
Autwped - Write the pedestal part of the data-sheet generation.
Autwnoi - Write the noise part of the data-sheet generation.
Autwgain - Write the gain part of the data-sheet generation.
Autwpeak - Write the peak part of the data-sheet generation.
Autwmisc - Write the miscellaneous part of the data-sheet generation.

The VI’s for reading the definition file

Autrfile - Main VI for reading the definition file, calls the ones below.
Autrhead - Reads the header of the definition file.
Autrgene - Read the general info for data-sheet generation.
A.4 Automatic testing

Auto.bias - Read the biasing part of the data-sheet generation.
Auto.ped - Read the pedestal part of the data-sheet generation.
Auto.noise - Read the noise part of the data-sheet generation.
Auto.gain - Read the gain part of the data-sheet generation.
Auto.peak - Read the peak part of the data-sheet generation.
Auto.misc - Read the miscellaneous part of the data-sheet generation.
Appendix B

Noise calculations for a readout system

Noise in read-out front-end electronics can be characterized in terms of common-mode noise and channel noise. For the channel noise one often use the two terms channel noise before and after common mode subtraction. The following calculation will show the relationship between these quantities.

B.1 Definitions

Each physical event, called e, of a total of $N_e$ events, is characterized by $N_i$ numbers, which are the $N_i$ data samples for the event. The samples for the event are read-out in parallel or serial, but usually confined to a 'small' amount of time. The i’th sample in the e’th event is denoted $d_i^e$.

The common mode for an event is defined as:

$$d^e = \frac{1}{N_i} \sum_{i=1}^{N_i} d_i^e$$  \hspace{1cm} (B.1)

The variation in common mode is usually induced on the system by external factors such as capacitive or inductive couplings to other electronics, and are not a part of the inherit noise contributions, which are unavoidable, in the readout system.

The average of common mode for all events is given by:

$$d = \frac{1}{N_e} \sum_{e=1}^{N_e} d^e = \frac{1}{N_e} \frac{1}{N_i} \sum_{e=1}^{N_e} \sum_{i=1}^{N_i} d_i^e$$  \hspace{1cm} (B.2)

The average of the i’th channel over all events (or possibly defined only for the events in this channel not containing a hit) is called the channels pedestal value, and is given by:

$$d_i = \frac{1}{N_e} \sum_{e=1}^{N_e} d_i^e$$  \hspace{1cm} (B.3)
The average of pedestals for all channels is also given by \( d \), seen by noting that the expression yields the same double sum as in B.2.

The common mode noise is defined as the standard deviation of \( d^e \) over all the events. This is given by

\[
\sigma^2(d) = \frac{1}{N_e} \sum_{e=1}^{N_e} (d^e - d)^2
\]  

(B.4)

The channel noise for channel \( i \) (calculated on raw data) is given as the standard deviation of the \( i \)’th channel over all the events.

\[
\sigma^2(d_i) = \frac{1}{N_e} \sum_{e=1}^{N_e} (d_i^e - d_i)^2
\]  

(B.5)

Common mode subtracted data differs from raw data in the sense that all raw data for this specific event has the common mode for this event subtracted. If primes denotes common mode subtracted data one then has:

\[
d_i^e = d_i^e - \bar{d}
\]  

(B.6)

The channel noise for common mode subtracted data is of course the same as in B.5 but with primed quantities replacing the unprimed

\[
\sigma^2(d_i^e) = \frac{1}{N_e} \sum_{e=1}^{N_e} (d_i^{e'} - d_i^e)^2
\]  

(B.7)

**B.2 Relationship between noise contributions**

In expression B.7 the right hand side can be expressed in terms of unprimed quantities by using B.6 and the fact that the average of a common mode subtracted channel is given by:

\[
d_i^e = \frac{1}{N_e} \sum_{e=1}^{N_e} d_i^e = \frac{1}{N_e} \sum_{e=1}^{N_e} (d_i^e - \bar{d}^e) = d_i - d
\]  

(B.8)

Writing B.7 using this yields

\[
\sigma^2(d_i^e) = \frac{1}{N_e} \sum_{e=1}^{N_e} ((d_i^e - d_i) - (\bar{d}^e - \bar{d}))^2
\]  

(B.9)

Performing the squaring yields then

\[
\sigma^2(d_i^e) = \frac{1}{N_e} (\sum_{e=1}^{N_e} (d_i^e - d_i)^2 - 2 \sum_{e=1}^{N_e} (d_i^e - d_i)(\bar{d}^e - \bar{d})) + \sum_{e=1}^{N_e} (\bar{d}^e - \bar{d})^2
\]  

(B.10)

Here the first and third term is easily recognized as \( \sigma^2(d_i) \) and \( \sigma^2(d) \), respectively. The total relationship on a channel basis is then.

\[
\sigma^2(d_i^e) = \sigma^2(d_i) + \sigma^2(d) - \frac{2}{N_e} \sum_{e=1}^{N_e} (d_i^e - d_i)(\bar{d}^e - \bar{d})
\]  

(B.11)
This equation is neither interesting nor helpful before it is summed over all i channels.

\[
\sum_{i=1}^{N_i} \sigma^2(d'_i) = \sum_{i=1}^{N_i} \sigma^2(d_i) + N_i \sigma^2(d) - \frac{2}{N_i} \sum_{i=1}^{N_i} (\sum_{i=1}^{N_i} (d'_i - d_i))(d' - d)
\] (B.12)

Here the inner sum in i in the last line is recognized as \(N_i(d' - d)\), which results in the fact that this term ends up being \(-2N_i \sigma^2(d)\), which yield the result

\[
\sum_{i=1}^{N_i} \sigma^2(d'_i) = \sum_{i=1}^{N_i} \sigma^2(d_i) - N_i \sigma^2(d)
\] (B.13)

If now a quantity called the average of the square of the noise over all channels are introduced as being

\[
\overline{\sigma^2(d_i)} = \frac{1}{N_i} \sum_{i=1}^{N_i} \sigma^2(d_i)
\] (B.14)

one finally obtains the compact result

\[
\overline{\sigma^2(d'_i)} = \overline{\sigma^2(d'_i)} + \sigma^2(d).
\] (B.15)

This states that the average of the square of the channel noise for raw data over all channels is equal to the same expression over common mode subtracted data plus the square of the common mode noise.
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